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Capacitor Condition Monitoring Based on the DC-Side Start-Up of Modular Multilevel Converters

Zhongxu Wang, *Student Member, IEEE*, Yi Zhang, *Student Member, IEEE*, Huai Wang, *Senior Member, IEEE*, and Frede Blaabjerg, *Fellow, IEEE*

Abstract—This paper proposes a new sub-module capacitor condition monitoring method for modular multilevel converters (MMCs) based on the DC-side start-up procedure. During this process, the MMC can be simplified into an RC charging circuit, and the sub-module capacitance can be estimated by investigating its relationship with the phase current and sub-module voltage. Several practical issues related to the implementation, advantages, and limitations of the proposed method are presented as well. In order to validate the method, a series of experiments with different sub-module capacitances are conducted based on a three-phase MMC platform. Experimental results confirm the effectiveness and feasibility of the proposed method.

Index Terms—Modular multilevel converters (MMCs), capacitor, condition monitoring.

I. INTRODUCTION

Modular multilevel converter (MMC) is one of the most promising topology candidates for high-voltage and high-power applications, where no series-connected power semiconductor devices are needed [1]. Apart from the power semiconductors, sub-module (SM) capacitors carry the arm current when the SM is inserted into the main circuit. Therefore, they play an essential role in the operation of the MMCs and have to be extremely reliable. In all types of capacitors, due to features like self-healing, excellent ripple current performance, and low equivalent series resistance [2]–[4], metalized polypropylene film (MPPF) capacitors are typically used in MMC applications. Although MPPF capacitors can provide better reliability performance, they are not failure-free. A 5% capacitance reduction is a common criterion for determining the end-of-life of the MPPF capacitor [5]. Thus, in order to enhance the availability of the whole MMC system and to schedule preventive maintenance, SM capacitor condition monitoring (CM) is necessary.

Plenty of CM methods have been proposed for DC-link capacitors in conventional two-level converters [5]. However, any hardware related approaches will add additional costs and introduce reliability issues to an MMC system when hundreds of SMs are involved. Thus, many CM methods designed for MMC are proposed based on advanced algorithms, such as Kalman filter [6], band-pass filter [7], and recursive least square algorithm [8]. All of them do not need additional hardware. However, they all make use of the SM voltage ripple, which is normally below 10% of the SM rated voltage. Regarding 5% value drop at the end-of-life of MPPF

capacitors, the voltage change used for condition monitoring accounts for merely 0.5% of the voltage sensor range. Only if the accuracy of voltage sensor is better than 0.5% (e.g., 0.3% or 0.1%), otherwise the above methods might fail to work with over 100% detection error. By contrast, by taking advantage of a particular characteristic of the MMC hardware topology, CM methods with special hardware implementation are proposed. Ref. [9] monitors the SM capacitance through an RC discharging circuit formed by an internal bleeding resistor. No extra measurement hardware or heavy computational load is needed in addition to a redundant SM in each arm. Moreover, larger SM voltage range is utilized with better monitoring accuracy. In [10], by introducing a reference SM, all other SM capacitances are able to be monitored by comparing its voltage ripple with the reference SM. The implementation of this method is easy and straightforward. However, the accuracy heavily depends on the voltage sensor accuracy and the power loading condition of the MMC.

In this paper, a novel condition monitoring method for SM capacitors is proposed based on an RC charging circuit during the DC-side start-up of the MMC. All SM capacitors can be monitored simultaneously with the information about the arm current and SM capacitor voltages, which are already available for common control purpose. The rest of this paper is structured as follows: Section II introduces the basic concept of the proposed CM method; Section III discusses the implementation of the proposed CM method followed by its advantages and limitations. The experimental validations are given in Section V. Section VI concludes the paper.

II. THE PROPOSED CONDITION MONITORING METHOD

Before the MMC gets into operation, all SM capacitors need to be charged to its rated voltage to avoid large inrush current. One straightforward way is to charge the capacitors from the DC-side of the MMC with a start-up resistor [11] as shown in Fig. 1(a). The RC network formed in this process offers an opportunity to do condition monitoring of the SM capacitors.

At the very beginning of the start-up, switches S_1 turns on and S_a turns off. An uncontrolled charging process occurs through the upper diode in the SM and the start-up resistor. The three-phase MMC thus can be simplified as Fig. 1(b). When focusing on the phase current and SM capacitor voltages in a specific phase, the three-phase MMC is equivalent to a single-phase circuit in Fig. 1(c) by tripling the start-up resistance. Since all diodes can be modeled by a constant voltage source V_d and an on-state resistor R_d [12], the circuit

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Z. Wang, Y. Zhang, H. Wang and F. Blaabjerg are with the Department of Energy Technology, Aalborg University, Aalborg, Denmark (e-mail: zho@et.aau.dk, yiz@et.aau.dk, hwa@et.aau.dk, fbl@et.aau.dk).

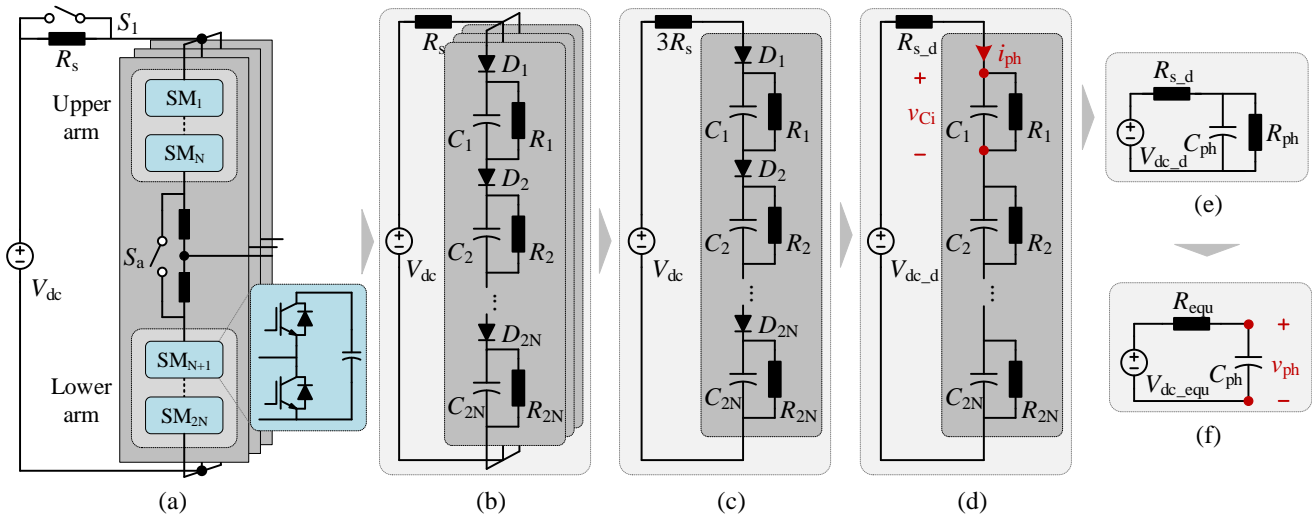


Fig. 1. Circuit simplification of the MMC during its start-up. (a) Three-phase MMC, (b) Equivalent three-phase MMC during DC-side start-up, (c) Equivalent single-phase MMC during DC-side start-up, (d) Equivalent single-phase MMC with linearized diode model, (e) Equivalent MMC circuit regarding the same phase current, and (f) Equivalent MMC circuit regarding the same phase capacitor voltage.

is then simplified into Fig. 1(d) and further into Fig. 1(e) with the parameters

$$\begin{cases} R_{s_d} = 3R_s + 2NR_d, V_{dc_d} = V_{dc} - 2NV_d \\ R_{ph} = \sum_{i=1}^{2N} R_i, \frac{1}{C_{ph}} = \sum_{i=1}^{2N} \frac{1}{C_i} \end{cases} \quad (1)$$

where R_{s_d} and R_s are the equivalent start-up resistance with/without considering the resistance of diodes; V_{dc_d} and V_{dc} are the equivalent DC bus voltage with/without considering the voltage drop from diodes; R_{ph} and C_{ph} are the equivalent phase resistance and capacitance; R_i and C_i are the resistance and capacitance of the i -th SM; N is the SM number per arm.

When seeing from the terminals of the equivalent phase capacitor C_{ph} in Fig. 1(e), its voltage v_{ph} can be derived as

$$\begin{cases} v_{ph} = V_{dc_equ} \left(1 - \exp\left(\frac{-t}{\tau_{equ}}\right) \right) \\ V_{dc_equ} = \frac{R_{ph}}{R_{ph} + R_{s_d}} V_{dc_d}, R_{equ} = \frac{R_{ph} R_{s_d}}{R_{ph} + R_{s_d}} \end{cases} \quad (2)$$

where V_{dc_equ} and R_{equ} are the equivalent DC voltage and resistance of the start-up circuit seeing from the terminals of C_{ph} ; $\tau_{equ} = R_{equ} C_{ph}$ is the equivalent time constant.

Therefore, the phase current i_{ph} can be calculated by

$$i_{ph} = \frac{V_{dc_d} - v_{ph}}{R_{s_d}} = \frac{V_{dc_d}}{R_{ph} + R_{s_d}} \left(1 + \frac{R_{ph}}{R_{s_d}} \exp\left(\frac{-t}{\tau_{equ}}\right) \right) \quad (3)$$

The phase current passes through all SMs connected in series in this phase, and the following current relationship holds for a specific SM as

$$C_i \frac{dv_{C_i}}{dt} + \frac{v_{C_i}}{R_i} = i_{ph}, \quad (4)$$

where v_{C_i} is the voltage across the i -th SM capacitor. By substituting (3) into (4), the SM voltage can be calculated as

$$\begin{cases} v_{C_i} = \left[A_1 R_i \left(1 - \exp\left(\frac{-t}{\tau_i}\right) \right) + \frac{A_2 \tau_{equ} R_i}{\tau_{equ} - \tau_i} \left(\exp\left(\frac{-t}{\tau_{equ}}\right) - \exp\left(\frac{-t}{\tau_i}\right) \right) \right] \\ A_1 = \frac{V_{dc_d}}{R_{ph} + R_{s_d}}, A_2 = \frac{R_{ph}}{(R_{ph} + R_{s_d}) R_{s_d}} V_{dc_d} \end{cases} \quad (5)$$

where $\tau_i = R_i C_i$ is the time constant of i -th SM. In practical MMC applications, τ_i is far larger (e.g., several thousand times) than τ_{equ} . It means that the transient voltage response of the SM capacitor is dominated by the smaller time constant τ_{equ} instead of τ_i . Therefore, in a short time period (e.g., several τ_{equ}), (5) can be rewritten as

$$\begin{cases} v_{C_i} = K_1 + \frac{K_2}{\tau_{equ} - \tau_i} \\ K_1 = A_1 R_i \left(1 - \exp\left(\frac{-t}{\tau_{rated}}\right) \right) \\ K_2 = A_2 \tau_{equ} R_i \left(\exp\left(\frac{-t}{\tau_{equ}}\right) - \exp\left(\frac{-t}{\tau_{rated}}\right) \right) \end{cases} \quad (6)$$

where $\tau_{rated} = R_{rated} C_{rated}$ is the time constant determined by the rated value of bleeding resistor and SM capacitor.

Thus, the SM capacitance can be calculated as

$$C_i = \frac{\tau_{equ}}{R_i} - \frac{K_2}{(v_{C_i} - K_1) R_i} \Big|_{t = n\tau_{equ}} \quad (7)$$

In order to clearly show how the SM capacitance is identified, the CM process is summarized as follows: 1) MMC is disconnected from the DC bus and AC grid. Meanwhile, all six arm inductors are bypassed by three switches to ensure no inductors interfere the start-up process; 2) Once all SM capacitors are discharged to zero voltage, S_1 turns on and the start-up begins; 3) MMC controller detects the maximum phase current I_{ph_max} and sets a timer to get the equivalent time constant τ_{equ} when the phase current drops to

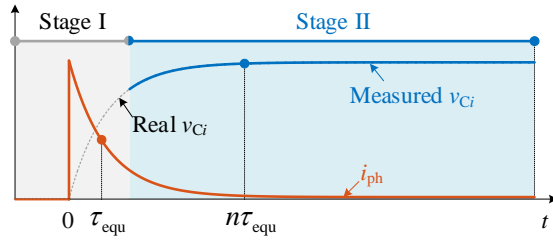


Fig. 2. Data sampling during the start-up process of the MMC.

$0.368I_{ph_max}$; 4) Measure all SM capacitor voltages when the timer counts to $n\tau_{equ}$ and calculate SM capacitance by (7).

III. PRACTICAL IMPLEMENTATION CONSIDERATIONS

In order to implement the proposed method, several practical issues need to be considered.

1) *Impact of Diode Tolerance and Degradation:* The constant voltage source V_d of the diode can be obtained from its data-sheet by curve-fitting, and all diodes share the same value. Since V_d is pretty small compared with the DC bus voltage, the impact of V_d change caused by the manufacturing tolerance and aging is negligible.

2) *R_{s_d} Measurement:* R_{s_d} can be updated at the beginning of each testing and thus no need to know the start-up resistance and the on-state resistance of the diodes. At the very beginning of the start-up process, all SM capacitors are in a short-circuit state. R_{s_d} can be calculated by the maximum phase current and DC bus voltage as

$$R_{s_d} = \frac{V_{dc_d}}{I_{ph_max}}. \quad (8)$$

3) *SM Voltage Measurement:* In case SM control board is powered by the SM capacitor [13], SM voltage v_{C_i} is only available after a period of time of start-up as shown in Fig. 2. In stage I, the SM controller is powered off and cannot send any data to the MMC central controller. In stage II, when the SM capacitor voltage exceeds a threshold, the SM control board is powered on and is able to measure the SM voltage for the capacitance estimation. Note that the phase current can be measured throughout the start-up process.

4) *Impact of Bleeding Resistor Tolerance:* The rated bleeding resistance is utilized in (6) instead of its real value. Thus, certain error might be introduced into the capacitance monitoring due to the bleeding resistor tolerance. Its impact is thus evaluated based on a 300 kV-300 MVA three-phase MMC system with 150 SMs per arm. Meanwhile, the following conditions are considered: 1) power dissipation of bleeding resistors accounts for 0.5% of the total power loss of the MMC system; 2) peak phase current during start-up is 10% of the maximum arm current of MMC; 3) SM capacitance is selected to ensure that the total energy storage in SM capacitors is about 30 kJ/MVA [14]. The following parameters can thus be obtained as: $R_{rated} = 2.4$ k Ω , $R_s = 1.0$ k Ω , and $C_{rated} = 5.0$ mF. By introducing $\pm 5\%$ variation to R_{rated} , its impact on the capacitance estimation can be evaluated and is shown in Fig. 3. It can be seen that the error is within 0.08%, which is extremely small and can be completely neglected.

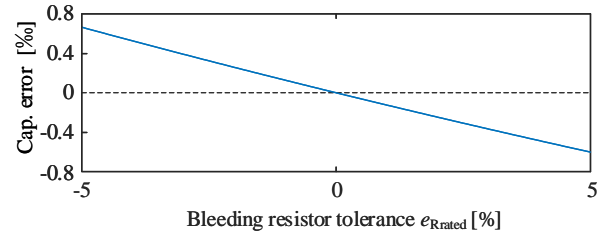


Fig. 3. The impact of bleeding resistor tolerance on capacitance estimation.

5) *Impact of Time Delay:* The time delay caused by signal sampling should be compensated if necessary. For example, the equivalent time constant τ_{equ} in practical MMCs is typically around several tens of milliseconds [14]. In this case study, τ_{equ} is equal to 0.05 s regarding the same selection requirements to the start-up resistor and SM capacitor mentioned above. Since it is calculated by detecting the phase current, considering a typical 20 kHz current sampling rate, a maximum 0.1% error will be introduced to τ_{equ} due to the current sampling delay of 0.05 ms.

IV. ADVANTAGES AND LIMITATIONS

Based on the above introduction to the proposed CM method, its main pros and cons are summarized as follows. The advantages are:

- The capacitance monitoring accuracy can be improved compared to other existing methods focusing on SM voltage ripple since half voltage sensor range is utilized.
- No additional measurement circuits, sensors, and auxiliary SMs are required. It means no extra reliability issues are introduced into the MMC system.
- All SM capacitances can be detected at one time and averaged by a series of results at different $n\tau_{equ}$ in order to mitigate the impact of measurement error.
- No impact is posed on the normal operation of the MMC since the whole CM process is done during the start-up.
- Complicated controls and calculations are not involved.

The limitations might be:

- Three switches are needed to bypass the arm inductors to exclude their impact on the phase current.
- The proposed method can only be conducted during the DC-side start-up of the MMC, which means that the SM capacitances cannot be monitored on-line and updated while the MMC is in operation. However, considering the very slow degradation rate of capacitors (e.g., in the units of month or year [15]), monitoring the SM capacitance during the shut-down of MMC system is still acceptable.

V. EXPERIMENTAL VALIDATION AND DISCUSSION

In order to verify the effectiveness of the proposed CM method, experiments are conducted based on a 15 kVA down-scaled three-phase MMC with four SMs per arm as shown in Fig. 4. The DC bus voltage is 900 V. The rated SM capacitance and bleeding resistance are 1.64 mF (two 820 μ F/400 V capacitors in parallel) and 12 k Ω , respectively. Several capacitors with smaller capacitances are connected in

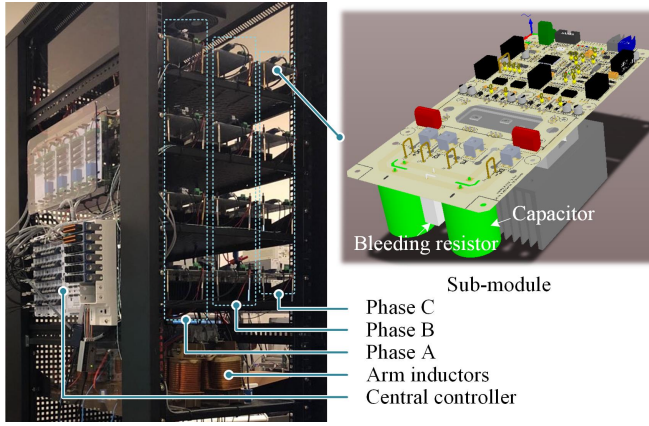


Fig. 4. Experimental platform (left) of three-phase MMC system including a sub-module overview (right).

TABLE I
COMBINATION OF CAPACITORS TO MIMIC THE SM DEGRADATION.

[uF]	C_{sm}	C_1	C_2	C_3	C_4	C_5	C_{sum}	%
C_{rated}	1640	10	10	22	22	22	-	-
Cap1	*	*	*	*	*	*	1716	0.00%
Cap2	*	*	*	*	*	*	1704	0.70%
Cap3	*	*	*	*	*	*	1694	1.28%
Cap4	*	*	*	*	*	*	1682	1.98%
Cap5	*	*	*	*	*	*	1672	2.56%
Cap6	*	*	*	*	*	*	1660	3.26%
Cap7	*	*	*	*	*	*	1650	3.85%
Cap8	*	*	*	*	*	*	1640	4.43%

parallel with the SM capacitor. By removing one or several of them, the SM capacitor aging is mimicked with 0% to approximately 4.5% value drop as listed in Table I. Due to the existence of manufacturing tolerance, which can be as large as $\pm 20\%$ for aluminum electrolytic capacitors, the real value of all capacitors are tested by an LCR meter and are shown in Table II for reference.

Experimental results with the phase current and SM voltage are shown in Fig. 5(a). It can be seen that, at the beginning of the start-up, the phase current rises sharply to the maximum value being about 4.8 A, then drops gradually to around zero. Meanwhile, the SM capacitor voltage increases and stabilizes at around 112.5 V. A series of experiments with different capacitances are conducted and the results are shown in Fig. 5(b) and (c). It can be seen that the higher the SM capacitance is, the lower the SM voltage is at the same time point. By substituting the measured SM voltages into (7), the value of SM capacitors can be measured.

Fig. 6 illustrates a comparison between the measured, rated and real SM capacitances. Compared with the rated capacitances, an constant monitoring error of around 10% can be observed from Fig. 7. By contrast, the monitoring error goes below 1% when compared with the real capacitance. It means that the 10% constant error mainly results from the capacitor manufacturing tolerance, whose average value is

TABLE II
THE RATED CAPACITANCES AND THE TESTED CAPACITANCES OBTAINED BY LCR METER AT 20 HZ.

	C_{sm1}	C_{sm2}	C_1	C_2	C_3	C_4	C_5
C_{rated} [uF]	820	820	10	10	22	22	22
C_{real} [uF]	731	732	9.9	9.8	20.4	20.3	20.5
Tolerance [%]	-10.9	-10.7	-1.0	-2.0	-7.3	-7.7	-6.8

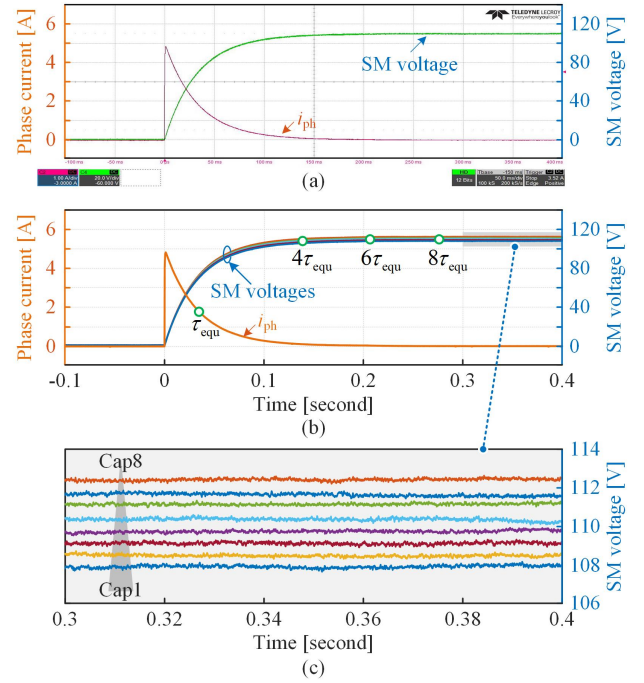


Fig. 5. Experimental results of phase current and SM voltage under different capacitor aging level (see Table I). (a) Experimental waveform from oscilloscope screen-shot; (b) SM voltages and phase current with different capacitors; (c) Zoom-in figure of SM voltages shown in (b).

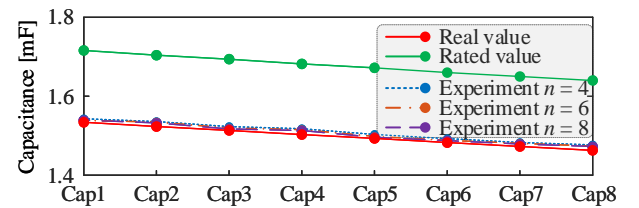


Fig. 6. Comparison among the measured, rated and real SM capacitances at different time points $n\tau_{equ}$ ($n = 4, 6, 8$) (see Fig. 5 (b)).

10.7% in this case study. Note that the manufacturing tolerance remains the same throughout the lifetime of capacitors. Since the capacitance change is regarded as the indicator of the capacitor's health status instead of the capacitance itself, the absolute value of capacitors are not necessary when it comes to condition monitoring. Therefore, given the constant error from manufacturing tolerance, the trends of the capacitance drop are shown in Fig. 9. It can be seen that the capacitance change percentage of the rated capacitance and real capacitance can be well captured by the proposed CM method, and they agree well with the change of both the rated and real values.

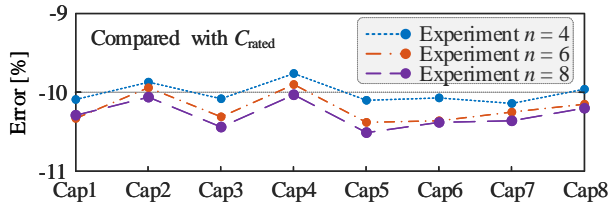


Fig. 7. Monitoring error compared with the rated capacitances.

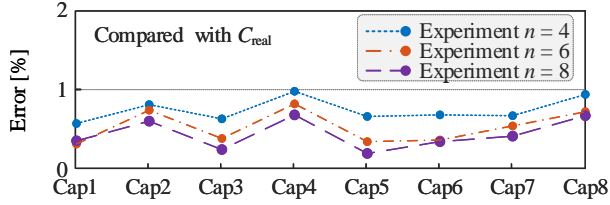


Fig. 8. Monitoring error compared with the real capacitances.

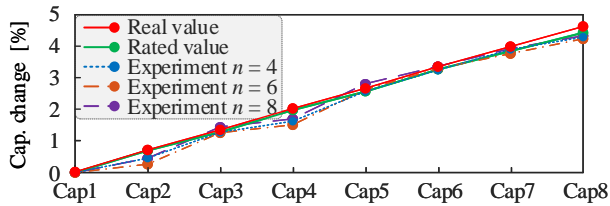


Fig. 9. Comparison of the capacitance change percentage between the measured, rated and real SM capacitances at different time points $n\tau_{eq}$ ($n = 4, 6, 8$).

VI. CONCLUSION

This paper has proposed a sub-module capacitor condition monitoring method based on the DC side start-up of the modular multilevel converter (MMC). By taking advantage of an RC charging network formed by the start-up resistor, the capacitance of SM capacitors can be estimated based on the phase current and SM voltage, which are already available for MMC control. The proposed method can monitor all SM capacitors at one time without additional sensors and heavy computational burden. A case study of a 15 kVA down-scaled MMC platform is presented. Experimental results show that the small capacitance change of SM capacitor can be monitored by the proposed method.

REFERENCES

- [1] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.
- [2] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters - An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep.-Oct. 2014.
- [3] Y. Tang, L. Ran, O. Alatis, and P. Mawby, "Capacitor Selection for Modular Multilevel Converter," *IEEE Trans. Ind. Appl.*, vol. 52, no. 4, pp. 3279–3293, Jul.-Aug. 2016.
- [4] L. Hui, Z. Meimei, Y. Ran, L. Wei, D. Jili, L. Haiyang, and Q. Haitao, "Reliability modelling and analysis on MMC for VSC-HVDC by considering the press-pack IGBT and capacitors failure," *J. Eng.*, vol. 2019, no. 16, pp. 2219–2223, Mar. 2019.
- [5] H. Soliman, H. Wang, and F. Blaabjerg, "A review of the condition monitoring of capacitors in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 52, no. 6, pp. 243–249, Nov. 2015.

- [6] O. Abushafa, S. Gadoue, M. Dahidah, and D. Atkinson, "A New Scheme for Monitoring Submodule Capacitance in Modular Multilevel Converter," in *Proc. 8th IET Int. Conf. Power Electron., Mach. Drives*, 2016, pp. 1–6.
- [7] D. Ronanki and S. S. Williamson, "Failure Prediction of Submodule Capacitors in Modular Multilevel Converter by Monitoring the Intrinsic Capacitor Voltage Fluctuations," *IEEE Trans. Ind. Electron.*, Early Access.
- [8] Y. J. Jo, T. H. Nguyen, and D. C. Lee, "Condition monitoring of submodule capacitors in modular multilevel converters," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, 2014, pp. 2121–2126.
- [9] H. Wang, H. Wang, Y. Zhang, Z. Wang, X. Pei, and Y. Kang, "Condition monitoring method for submodule capacitor in modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10403–10407, Nov. 2019.
- [10] F. Deng, Q. Wang, D. Liu, Y. Wang, M. Cheng, and Z. Chen, "Reference submodule based capacitor monitoring strategy for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4711–4721, May 2019.
- [11] B. Li, D. Xu, Y. Zhang, R. Yang, G. Wang, W. Wang, and D. Xu, "Closed-loop precharge control of modular multilevel converters during start-up processes," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 524–531, Feb. 2015.
- [12] Y. Zhang, H. Wang, Z. Wang, Y. Yang, and F. Blaabjerg, "Simplified Thermal Modeling for IGBT Modules with Periodic Power Loss Profiles in Modular Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2323–2332, Mar. 2018.
- [13] T. Modeer, S. Norrga, and H. P. Nee, "High-voltage tapped-inductor buck converter auxiliary power supply for cascaded converter submodules," in *Proc. IEEE Energy Convers. Congr. Expo.*, IEEE, 2012, pp. 19–25.
- [14] K. Ilves, S. Norrga, L. Harnefors, and H. P. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 77–88, Jan. 2014.
- [15] Y. Wu and X. Du, "A VEN Condition Monitoring Method of DC-Link Capacitors for Power Converters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 2, pp. 1296–1306, Feb. 2019.